WHAT IS CLAIMED IS:

1. A method of error correction in a high-speed data transmission system, comprising:

   determining a value of an input signal at a decision timeframe and holding the value as a tentative value;

   estimating an error of the value, amplifying the error of the value, and holding the amplified error of the value as a corrected value;

   deciding if the amplified error of the value is within a defined marginal range;

   determining if the input signal is involved in a transition from a positive to negative state or from a negative to positive state during a symbol period; and

   correcting the tentative value to the corrected value if both the error of the value is in the defined marginal range and the input signal is involved in the transition.

2. A method of error correction in a high-speed data transmission system according to claim 1, wherein two adjacent values of the input signal are calculated before and after the decision timeframe to determine if the input signal is involved in a transition.

3. A method of error correction in a high-speed data transmission system according to claim 2, wherein the two adjacent values are calculated one-half a symbol period before and after the decision timeframe.

4. A method of error correction in a high-speed data transmission system according to claim 3, wherein the two adjacent values are involved in a transition from less than – 0.75, to greater than + 0.75 or from greater than + 0.75 to less than –0.75.

5. A method of error correction in a high-speed data transmission system according to claim 3, wherein the two adjacent values are involved in a transition from – 1 to + 1, or from +1 to –1.

6. A decision system in high-speed data transmission, comprising:

a data decision circuit to determine a value of an input signal at a decision instance and to hold the value as a tentative value;

an error estimator module to determine an error value of the value, to amplify the error value, and to hold the amplified error value as a corrected value;

an error verifier module to determine whether the amplified error value is within a marginal range;

a transition detecting module, to determine whether the input signal was in transition from a positive to negative state, or a negative to positive state during a symbol period; and

an error correction module to determine whether the tentative value should be overridden by the corrected value.

7. The decision system according to claim 6, wherein the error verifier module includes an absolute value circuit to make the error value a positive number and a comparator to compare the error value to a reference value.

8. The decision system according to claim 6, wherein adjacent sample values of the input signal before and after the decision instance are used to determine if the input signal is in transition.

9. The decision system according to claim 8, wherein the adjacent samples values are calculated one-half a symbol period before and after the decision instance.

10. The decision system according to claim 8, wherein the transition detecting module includes an adder to add the adjacent sample values, an absolute value circuit to make positive the added adjacent sample values, and a comparator to compare the added adjacent sample values to a reference value.

11. A receiver utilized in high speed data transmission to output data values, comprising:

an analog-to-digital converter to receive an input signal and to output a sampled digital signal and a phase information;

a decision system to receive the sampled digital signal and to output a value from the receiver, wherein the decision system:

receives the sampled digital signal, calculates a value at a decision instance, and assigns a tentative value;

calculates an error value, amplifies the error value and holds it as a corrected value;

determines if the error value is within a marginal range;

determines whether the input signal was in a transition from a positive to negative state, or a negative to positive state during a symbol period; and

outputs the corrected value as the value if the error value is within the marginal range and if the input signal is in a transition during a symbol period;

a phase detector to receive the value and the phase information and to output a detected phase information;

a loop filter to receive the detected phase information and to output a filtered phase information; and

an oscillator to receive the filtered phase information and to output a clock signal as a sampling clock for the analog-to-digital converter.

12. The receiver according to claim 11, wherein adjacent sample values of the input signal before and after the decision instance are used to determine if the sampled digital signal is within a transition.

13. The receiver according to claim 12, wherein the adjacent sample values are calculated one-half a symbol period before and after the decision instance.

14. The receiver according to claim 11, wherein the decision system includes:

a data decision circuit to receive the sampled digital signal, to calculate a value at a decision instance, and to assign the tentative value;

an error estimator module to calculate an error value, to amplify the error value and to hold it as the corrected value;

an error verifier module to determine if the error value is within a marginal range;

a transition detecting module to determine whether the sampled digital signal was in a transition from a positive to negative state, or a negative to positive state during a symbol period; and

an error correction module to output the corrected value as the value if the error value is within the marginal range and if the sampled digital signal is involved in a transition.

15. The receiver according to claim 14, wherein the error verifier module includes an absolute value circuit to make the error value a positive number and a comparator to compare the error value to a reference value.

16. The receiver according to claim 14, wherein the transition detecting module includes an adder to add the adjacent sample values, an absolute value circuit to make positive the added adjacent sample values, and a comparator to compare the added adjacent sample values to a reference value.

17. The system receiver according to claim 11, wherein the input signal is received from a T1 data transmission system.

18. The system receiver according to claim 17, wherein the T1 data transmission system includes a plurality of cascaded T1 links.

19. A decision circuit, comprising:

a machine-readable storage medium; and

machine-readable program code, stored on the machine readable storage medium, the machine-readable program code having instructions to

calculate a value of an input signal at a decision instance and to hold the value as a tentative value,

calculate an error value, amplify the error value, and hold the amplified error value as a corrected value,

determine whether the error value is within a marginal range,

determine the input signal was in transition from a positive to negative state, or from a negative to positive state during a symbol period, and

decide whether the tentative value should be overridden by the corrected value.

20. The decision circuit according to claim 19, wherein adjacent sample values of the input signal before and after the decision instance are used to determine if the input signal is in transition.

21. The decision circuit according to claim 20, wherein the adjacent sample values of the input signal are calculated one-half a symbol period before and after the decision instance.